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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,445	09/20/2004	Jason Chen	12295-US-PA	5444

31561 7590 04/27/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
GOODWIN, DAVID J	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,445	CHEN ET AL.	
	Examiner	Art Unit	
	David Goodwin	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 through 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (US 6165842) in view of Ueda (US 6090666).

3. Regarding claims 1 and 12.

4. Shin teaches a method of making a floating gate transistor. Said method comprises forming a tunnel oxide layer (304) over a substrate (302). Forming an amorphous silicon charge storage layer (310) over the tunnel oxide layer (304) (column 3 lines 27-37). The silicon charge storage layer (310) is partially oxidized to form a plurality of nanocrystals (314) overlain by a layer of oxide (fig 3e) (column 3 lines 35-45). Intergate dielectric (316) is formed over the nanocrystal layer (fig 3g) (column 3 lines 45-50. A control gate (318) is formed over the integrate dielectric layer (316) and used as a mask in patterning the staked structure of the floating gate comprising a tunnel oxide layer (304), a floating gate layer (316) an integrate dielectric layer (316) and a control gate layer (318). Source and drains regions (324) are then implanted into the substrate (fig 3j) forming a flash memory device (fig 3k) (column 3 lines 45-57).

5. Shin does not teach that the oxidized portions of the charge storage layer may comprise part of the integrate dielectric.

6. Ueda teaches a method of making a flash memory device. The method comprises. Forming a plurality of nanocrystals (13) over a substrate (11). The surface of the nanocrystals is then oxidized (fig 2c) forming an oxide (14a) that comprises a portion of the integrate dielectric (fig 2d) (column 12 lines 20-45).

7. It would have been obvious to one of ordinary skill in the art to use the oxide formed over the nanocrystals as integrate dielectric in order to minimize the number of process steps and to assure a high quality gate interface.

8. Further Shin does not teach that the oxidation of the charge storage layer is a thermal process

9. Ueda teaches that the oxidation of silicon is carried out under thermal conditions (column 9 lines 1-10).

10. It would have been obvious to one of ordinary skill in the art that the oxidation of silicon would be undertaken at thermal conditions in order that oxide is formed at a reasonable rate.

11. Regarding claim 2, 3, 4, and 5.

12. Ueda further teaches that the nanocrystals (13) may be made from silicon, germanium, or a combination thereof (column 15 lines 10-20).

13. It would have been obvious to use silicon, germanium, or a combination thereof in order to physical and electrical characteristics of the nanocrystals and the properties of the floating gate transistor formed therewith.

14. Regarding claims 6 and 11.

15. Ueda further teaches that an amorphous layer of silicon, which will be converted into nanocrystals may be formed using the low pressure chemical vapor deposition of silicon from monosilane (SiH4) gas at 500 degrees C. The low pressure state is maintained at 0.01 Torr during the deposition and subsequent treatment (column 9 lines 10-30).

16. It would have been obvious to one of ordinary skill in the art to deposit a silicon layer for subsequent use as a charge storage layer using LPCVD of monosilane gas at 0.01 Torr in order to deposit a high quality silicon layer for subsequent processing.

17. Regarding claim 7.

18. Ueda further teaches that the oxidation of silicon may comprise a rapid thermal oxidation (column 9 lines 5-10).

19. It would have been obvious to one of ordinary skill in the art to use a rapid thermal process to oxidize the surface of silicon in order to maintain high process throughput and control of the depth to which the silicon is oxidized.

20. Regarding claims 8 and 9.

21. Ueda further teaches that the oxidation of silicon may comprise a rapid thermal oxidation under atmosphere comprising N20 and O2 (column 9 lines 5-10).

22. It would have been obvious to one of ordinary skill in the art to oxidize under an atmosphere comprising N20 and O2 in order to supply oxygen to the surface of the silicon for subsequent oxidation of the silicon.

23. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (US 6165842) in view of Ueda (US 6090666).

24. Shin in view of Ueda teaches all elements of the claimed invention above.

25. Shin in view of Ueda does not teach that the rapid thermal oxidation of silicon under an atmosphere comprising oxygen may be undertaken at between 850 and 1000 degrees C.

26. It would have been obvious to one of ordinary skill in the art that an rapid thermal oxidation at 1050 degrees is close to the range of 850 to 1000 degrees and that the temperature of the process may be adjusted down to 1000 degrees to marginally reduce the rate of oxidation and thereby increase the control of the process.

Response to Arguments

27. Applicant's arguments filed 03/09/2006 have been fully considered but they are not persuasive.

28. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

29. In response to the applicant's argument that that Shin does not teach the thermal oxidation of a portion of the charge storage layer to form the interlayer dielectric while the remaining portion becomes the charge storage layer. Shin teaches the oxidation,

always a thermal process, of a portion of the charge storage layer forming an overlying layer of oxide on the remaining portion of nanocrystaline material which becomes the charge storage layer. It would have been odious in view of Uedo, as explained above, that the oxidized material can comprise at least a portion of the interlayer dielectric layer.

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Goodwin whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJG

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